ABSTRACT

A semiconductor memory device having a dummy memory cell and a reading method of the same, wherein provision is made of a memory cell 11 connected to a word line WL and a pair of bit lines BL and xBL, a dummy memory cell 12 connected to a word line WL and a pair of dummy bit lines DBL and xDBL, and a word line driver 13 for activating the word line at a common timing, and when the data is read out from the memory cell, a timing of the reading of the data is determined in accordance with a level of the dummy bit lines connected to the dummy memory, and when a voltage difference of a pair of dummy bit lines becomes a threshold voltage, the word line driver deactivates the word line and precharges the dummy bit lines.